

ECS Configuration Change Request

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1. Originator Rajesh Dharia	2. Log Date: 1/19/00	3. CCR #: 00-0062	4. Rev:	5. Tel: x0498	6. Rm #: 3204E	7. Org. DevEng
8. Title of Change: Install Higher-speed CPUs in pdps2 with additional memory to Support IRR DPS Benchmarking						
9. Originator Signature/Date <i>Rajesh Dharia 1/19/00</i>		10. Class II	11. Type: CCR	12. Need Date: 1/20/		
13. Office Manager Signature/Date <i>AA 1-19-00</i>		14. Category of Change: EDF		15. Priority: (If "Emergency" fill in Block 28). Emergency		
16. Documentation/Drawings Impacted: N/A		17. Schedule Impact: Low		18. CI(s) Affected: DPS/PRONG		
19. Release Affected: None 6A		20. Date due to Customer: N/A		21. Impl. Date: 1/20/2000		22. Estimated Cost: None
23. Source Reference: <input type="checkbox"/> NCR (attach) <input type="checkbox"/> Action Item <input type="checkbox"/> Tech Ref. <input type="checkbox"/> GSFC <input checked="" type="checkbox"/> Other: Steve Fox and Joe Guzek recommended to expedite this in preparation for IRR DPS bench marking.						
24. Description of Change: (use additional Sheets if necessary) Temporarily install higher-capacity ultra 3000 CPUs into pdps2 with additional 1 GB memory. The CPUs will remain in the machine until benchmarking is complete for DPS for IRR, about 1/29. This work will be performed by EDS Robert Bymes. RTSC personal should be available to bring this machine down tomorrow morning at 7:00 am.						
25. Proposed Solution: (use additional sheets if necessary) Install 1 cpu memory board from machine sahara (EIN # 3271) with 512 Meg memory into PDPS2 (EIN # 4664). Install additional power supply from EDS inventory (Robert Bymes has already kept aside). Remove 2 167 Mhz CPUS from PDPS2 and install 4 CPUS. Total PDPS2 machine will have 4 CPUS with 1GB memory. This work will be done by EDS Robert Bymes on Thursday morning beginning at 7:00 am. Total down time will be 1 hour max.						
26. Alternate Solution: (use additional sheets if necessary) None						
27. Consequences if Change(s) are not approved: (use additional sheets if necessary) DPS will not be able to justify how we are going to meet the performance goals of 6A, and so may fail the IRR on 1/31/2000.						
28. Justification for Emergency (If Block 15 is "Emergency"): The slides for the IRR must be in by 1/26, so the benchmarking must be completed within the next week, and must start now.						
29. Site(s) Affected: <input checked="" type="checkbox"/> EDF <input type="checkbox"/> Mini-DAAC <input type="checkbox"/> VATC <input type="checkbox"/> EDC <input type="checkbox"/> GSFC <input type="checkbox"/> LaRC <input type="checkbox"/> NSIDC <input type="checkbox"/> SMC <input type="checkbox"/> AK <input type="checkbox"/> JPL <input type="checkbox"/> EOC <input type="checkbox"/> IDG Test Cell <input checked="" type="checkbox"/> Other Development Functionality Lab						
30. Board Comments:				31. Work Assigned To:		
32. EDF/REL2 CCB Chair (Sign/Date): <i>Robert Bymes 1/19/00</i>		33. Disposition: <u>Approved</u> A/C Disapproved Fwd/ECS Fwd/ESDIS		34. (TBD)		
35. M&O CCB Chair (Sign/Date):		36. Disposition: Approved A/C Disapproved Fwd/ECS Fwd/ESDIS		37. CM Manager's Closure:		
38. ECS CCB Chair (Sign/Date):		39. Disposition: Approved A/C Disapproved		40. CCR Closed Date:		

CM01 March 8, 1999

ORIGINAL

ECS/EDF/REL2 CCB
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